INTERSIL

Designing Low Power 12 Bit Microprocessor Systems

The first stage in designing battery operated microprocessor systems is to define clearly the tasks which the microprocessor must perform and the time in which these tasks must be accomplished. One must also select the appropriate microprocessor.

With low power the goal, only a CMOS microprocessor should be considered, as it is only CMOS which is capable of providing real low power operation. There are essentially three different types of CMOS microprocessor: 4-bit devices, such as TI's CMOS version of their TMS1000; 8-bit devices, such as the CDP1802 COSMAC, RCA's single-chip derivative of their CDP1804, and Intersil's CMOS equivalent of Intel's MCS48 family; and 12-bit devices, such as Intersil's IM6100.

Since power is consumed principally in charging and discharging circuit nodes, the key to lowest power consumption in CMOS is to run as slowly as possible. Therefore the microprocessor of choice is the one which performs the required tasks with the minimum number of clock cycles (instruction steps). This is affected primarly by word length, architecture and I/O structure.

Word length has a two pronged effect. First the word length must be adequate for the data to be handled. For example, if it is desired to work with data to a precision of 0.1%, a 4 or 8-bit processor would have to operate in multiple precision while a 12-bit device can operate in single precision. (0.1% corresponds to 10 bits). Going from single to double precision always more than doubles the number of instructions required.

Word length also affects instruction coding efficiency. In the IM6100, 12-bit processor memory reference instructions contain the instruction and referred address in one word, which is fetched in one machine cycle. 8-bit processors must either use two or more words for direct or indirect memory reference instructions or resort to using CPU registers as pointers. This, however, involves overhead in loading the pointers, and therefore 12-bit microprocessor may prove appropriate even when only 8-bit data is to be handled.

Architecture should be the next consideration when selecting a low power microprocessor. Different architectures have different efficiencies when applied to the same operation, and it is desirable to benchmark typical program segments on alternative machines before making a final choice, as these differences can be significant, and a processor using only half the instructions for a certain task can perform that task at reduced power.

Attention should also be given to the choice of I/O structure; for example, DMA should be examined if fast, large volume I/O is necessary. Another important consideration is the ease with which the microprocessor can test single input bits or set and clear output bits. It is often at this point that the hardware/software tradeoff shows up. For example, using sofware, it is clearly possible to set and clear individual I/O bits by writing complete new parallel words to an output port, however this can be somewhat cumbersome. The IM6100 hardware solution is shown in fig. 1. In this case any one of 8 bits can be set or cleared by a single I/O instruction. The choice of software or hardware is determined by calculating the differences in current drawn by each option.

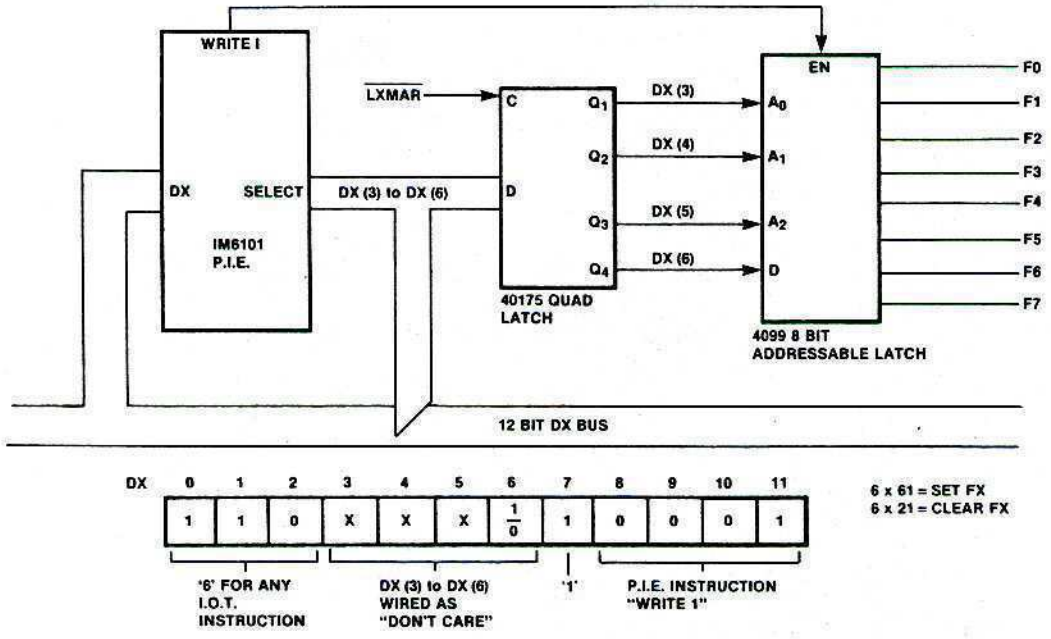


Figure 1. Hardware for setting and clearing individual bits of an IM 6100 output port

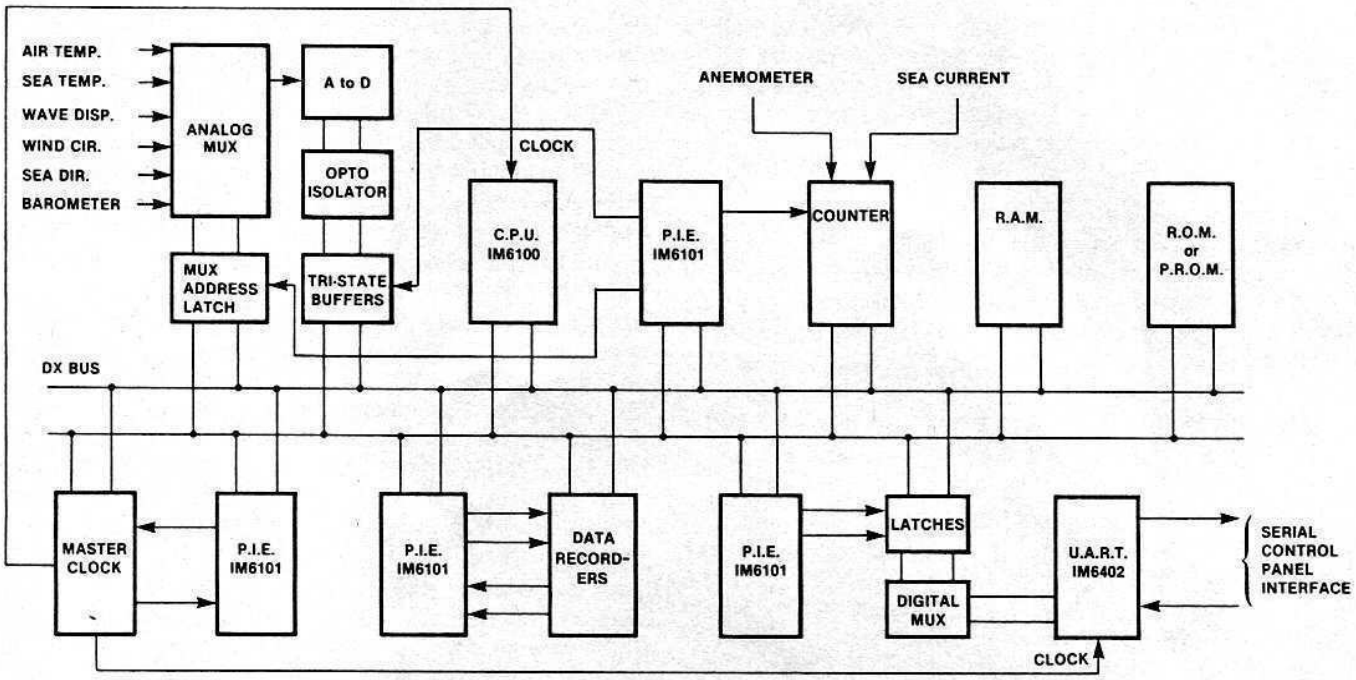


Figure 2. Block diagram of oceanographic data buoy. The master clock (bottom left) is controlled by an output from the adjacent P.I.E.

In many microprocessor applications demands on the processor are uneven, with long, relatively idle periods being interspersed with busy activity. Under these circumstances it is beneficial to reduce the clock frequency or even stop the clock entirely during those periods of inactivity. (Most CMOS microprocessors are static, therefore there is no minimum clock frequency). Figure 2 shows the block diagram of an oceanographic data buoy which acquires data at a slow rate then has a burst of activity as data is analyzed and transferred to tape. The dual frequency clock is controlled by a flag output from the IM6101 PIE, and the entire system, including the recorders, draws only 2.5mA from a 12V battery supply.

If a large memory is used it is desirable to access only those devices which are addressed at any one time. Memories consume their lowest amount of power when not being accessed, and by decoding high order address bits the enable strobes can be gated only to those memories currently addressed, with the others left in their low power mode. (See fig. 3).

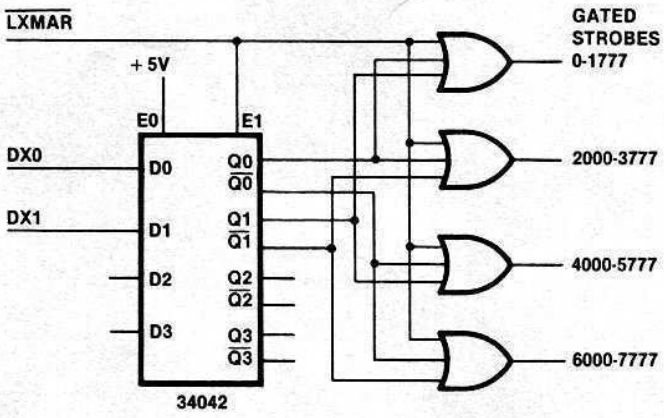


Figure 3. Selection of 1K memory banks by gating strobe to each bank

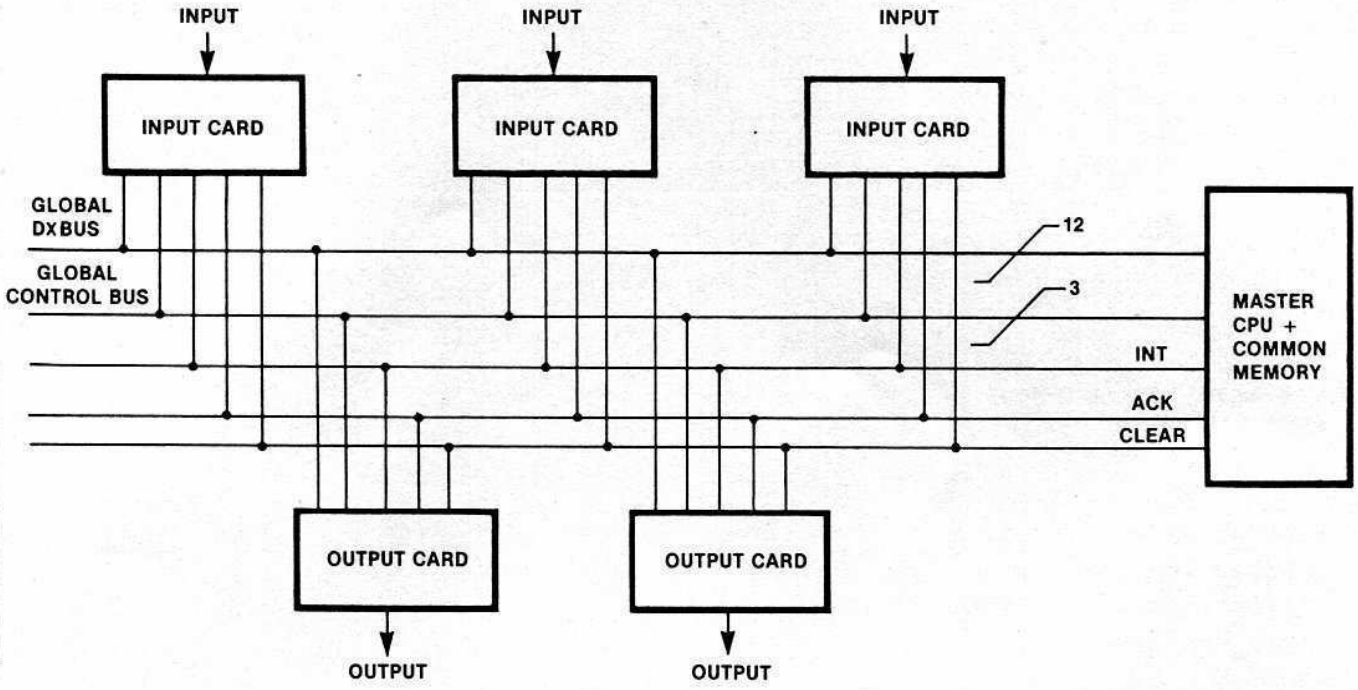


Figure 4. Multiprocessor Meteorological Station

One point worth noting is that adding hardware in a CMOS system does not necessarily increase power consumption, and may in fact be advantageous. Figure 4 shows the block disgram of a multi-processor meteorlogical station in which there are individual processors for each input and output channel, and a common memory area attached to a master processor as a "mail box" for data. This arrangement considerably simplifies the writing of software, as a change in I/O channel does not have repercussions throughout the whole system. One microprocessor might be capable of handling all tasks, but it would have to run at a much higher clock frequency, and therefore consume the same power as the sum of the individual processors.

Finally, the intelligent use of interrupts can save power as there is no need for wait loops and skip chains. The IM6100, together with the IM6101PIE, provides a complete, prioritized, vectored multilevel interrupt system which can save a lot of software time. Figure 5 lists the IM6100 family devices together with their principal features.

IM 6100	-	12 bit C.P.U.
IM 6101	-	Parallel Interface Element Vectored Interrrupt Controller
IM 6102	-	Memory Extender Simultaneous DMA Controller Real Time Clock
IM 6103	-	20 bit I/O port
IM 6312	-	1024 x 12 ROM
IM 6402/3	-	Universal Asynchronous Receiver/Transmitter
IM 6508/18	-	1024 x 1 RAM
IM 6512	-	64 x 12 RAM
IM 6551/61	-	256 x 4 RAM
IM 6653	-	1024 x 4 EPROM
ICL 7109	-	12 bit A to D converter
ICL 7112	-	12 bit D to A converter
ICM 7211	-	4 digit L.C.D. display driver
ICM 7212	-	4 digit L.E.D. display driver
ICM 7218	-	8 digit L.E.D. display driver

Figure 5. The IM 6100 Microprocessor Family.

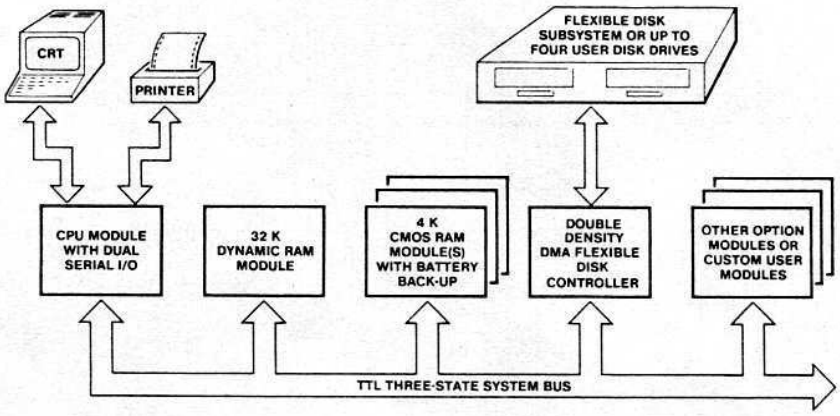
INTERSIL

M009

LSI-8 OEM Microcomputer System

FEATURES

- Low cost
- Powerful PDP®-8/e compatible processor
- Compact size
- Modular design
- Expandable memory (to 32K words)
- Bus supports easy I/O expansion
- Resident firmware monitor/debugger
- Large available software base
- Low power
- Supports interrupt and DMA operations



LSI-8 SYSTEM BLOCK DIAGRAM

GENERAL DESCRIPTION

Intersil's LSI-8 OEM microcomputer system is a general purpose computer which executes PDP®-8/e software. It is ideally suited to applications requiring a powerful, reliable, easily serviced computer system. It's small size, extensive options, and low power requirements allow tailoring to a broad range of uses.

The LSI-8 is a complete system with a feature-packed CPU, many I/O and memory options, and several physical configurations. It is available as a fully configured "turn-key" system (also known as Intercept III) or as a set of modules configurable by the user.

A three-state, multi-slot TTL bus allows system expansion to the full memory and I/O capacity.

As a complete pre-packaged system, the LSI-8 provides a low-cost solution to medium volume application problems such as small business computers, office computers, inventory management systems, laboratory systems, etc.

For high volume applications, all LSI-8 components and modules are available separately at very competitive prices. Applications include dedicated process control systems, remote data acquisition systems, instrument control systems, etc.

Regardless of the configuration, Intersil's LSI-8 system provides a flexible and reliable solution to applications requiring low cost, high performance and fast delivery. Many options are available, and all systems and modules are shipped fully tested with documentation and schematics. PDP®-8/e software compatibility means software is available from hundreds of existing sources or easily developed using the mature development tools available.

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